TITLE

THIN FILM TRANSISTOR AND METHOD FOR FABRICATING THE SAME

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for *THIN FILM TRANSISTOR AND METHOD OF FABRICATING THE SAME* earlier filed in the Korean Intellectual Property Office on 17 April 2003 and there duly assigned Serial No. 2003-24431.

BACKGROUND OF THE INVENTION

Field of the invention

[0002] The present invention relates to a thin film transistor and a method for fabricating the same, more particularly, to a thin film transistor for preventing short of circuit due to step and a method for fabricating the same.

Description of Related Art

[0003] Recently, thickness of gate insulation layer of a thin film transistor is gradually reduced. However, frequency of short generation between activation layer and gate electrode is increased as thickness of the gate insulation layer on the side wall of the activation layer is being reduced due to

a high step generated as buffer layer in the lower part of the activation layer is etched at the same when the activation layer is formed.

[0004] The earlier art is described in detail as follows.

[0005] A polysilicon layer is formed by crystallizing an amorphous silicon layer deposited on a glass substrate equipped with buffer layer. Then, an activation layer is formed by patterning the polysilicon layer, and surface treatment process is performed using HF, *etc.*, to remove impurities on the surface of the activation layer.

[0006] Next, a gate insulation layer is deposited on the substrate, and a gate electrode is formed on the gate insulation layer.

[0007] A step A1 is formed on the buffer layer accordingly since the buffer layer is over-etched in patterning process for forming the activation layer and surface treatment process for treating the surface of the activation layer.

[0008] It can be seen that thickness of the gate insulation layer on the side wall of the activation layer is reduced by the high step A1 formed by over-etching of the buffer layer. That is, it can be seen that thickness of the gate insulation layer on the side wall of the activation layer is reduced from B1 to B2. Therefore, a short can be generated between the activation layer and gate electrode as thickness of the gate insulation layer is reduced.

[0009] There is a method for forming the gate insulation layer thickly in order to solve the foregoing problems. However, there are problems in that driving voltage is increased, and power consumption is increased if the gate insulation layer is deposited thickly.

SUMMARY OF THE INVENTION

[0010] Therefore, in order to solve the foregoing problems of the earlier art, it is an object of the present invention to provide a thin film transistor capable of preventing short of circuit by controlling step formed during formation of activation layer and preventing deterioration of efficiency or generation of display defects by decreasing thickness of gate insulation layer and a method for fabricating the thin film transistor.

[0011] It is another object to provide a thin film transistor in which a short is not generated between the activation layer and gate electrode by forming gate insulation layer to an even thickness on the side wall of the activation layer in case that the step is formed in a height corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer.

[0012] It is yet another object of the present invention to provide a thin film transistor capable of forming gate insulation layer more thinly and controlling thickness of activation layer also in advance by controlling the step.

[0013] It is still another object of the present invention to provide a thin film transistor that is easy and inexpensive to manufacture and yet more reliable.

[0014] It is another object to provide a thin film transistor capable of preventing a short of a circuit while not increasing driving voltage and power consumption.

[0015] In order to achieve the foregoing and other objects, the present invention provides a thin film transistor including a buffer layer formed on glass substrate; an activation layer formed on the buffer layer; and a gate insulation layer formed on the buffer layer including the activation layer, wherein the buffer layer has a step formed between a lower part of the activation layer and a part

except the lower part of the activation layer, and the step is a half or less of the thickness sum of the activation layer and gate insulation layer.

[0016] It is preferable that the buffer layer has a step to such a degree that thickness of the gate insulation layer is not changed on the side wall of the buffer layer. Furthermore, it is preferable that thickness of the gate insulation layer is 400 Å (Angstroms) or more in case that thickness of SPC polysilicon is 300 Å and step is 350 Å in the activation layer, and thickness of the gate insulation layer is 1,000 Å or more in case that thickness of ELA polysilicon is 500 Å and step is 750 Å in the activation layer.

[0017] Furthermore, the present invention provides a method for fabricating a thin film transistor including the steps of depositing an amorphous silicon layer on glass substrate equipped with buffer layer; forming a polycrystalline silicon layer by crystallizing the amorphous silicon layer; forming an activation layer by etching the polycrystalline silicon layer; treating the surface of the activation layer; and depositing a gate insulation layer on the substrate, wherein etching time is controlled in the activation layer forming process and activation layer surface treatment process so that step between a lower part of gate in the buffer layer and a part except the lower part of the gate has a step value corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer.

[0018] In preferred embodiments of the present invention, it is preferable that the etching time is controlled so that the buffer layer has a step to such a degree that thickness of the gate insulation layer is not changed on the side wall of the buffer layer, and the buffer layer has a step corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0020] FIG. 1 is a cross sectional view illustrating a conventional thin film transistor;

[0021] FIG. 2 is a SEM photograph showing that short is generated at the side surface of activation layer by over-etching in the conventional thin film transistor; and

[0022] FIG. 3 is a thin film transistor according to one preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] Turning now to the drawings, FIG. 1 is a cross sectional view illustrating a conventional thin film transistor and FIG. 2 is a SEM photograph showing that a short is generated at the side surface of activation layer by over-etching in the conventional thin film transistor.

[0024] Referring to FIG. 1, a polysilicon layer is formed by crystallizing an amorphous silicon layer deposited on a glass substrate 100 equipped with buffer layer 110. Then, an activation layer 120 is formed by patterning the polysilicon layer, and surface treatment process is performed using HF, *etc.*, to remove impurities on the surface of the activation layer 120.

[0025] Next, a gate insulation layer 130 is deposited on the substrate, and a gate electrode 140 is formed on the gate insulation layer.

[0026] A step A1 is formed on the buffer layer 110 accordingly since the buffer layer 110 is over-etched in patterning process for forming the activation layer 120 and surface treatment process for treating the surface of the activation layer 120.

[0027] Referring to FIG. 2, it can be seen that thickness of the gate insulation layer 130 on the side wall of the activation layer 120 is reduced by the high step A1 formed by over-etching of the buffer layer 110. That is, it can be seen that thickness of the gate insulation layer on the side wall of the activation layer is reduced from B1 to B2 as illustrated in FIG. 2. Therefore, a short can be generated between the activation layer 120 and gate electrode 140 as thickness of the gate insulation layer 130 is reduced.

[0028] There is a method for forming the gate insulation layer 130 thickly in order to solve the foregoing problems. However, there are problems in that driving voltage is increased, and power consumption is increased if the gate insulation layer 130 is deposited thickly.

[0029] The present invention will now be described in detail in connection with preferred embodiments with reference to the accompanying drawings. For reference, like reference characters designate corresponding parts throughout several views.

[0030] FIG. 3 is a thin film transistor according to one preferred embodiment of the present invention. As seen in Figs. 1-3, each one of the steps A1 and A2 is a distance until a top of the buffer layer overstretched from top of the activation layer. In addition, the degree of the step is the height of the step.

[0031] Referring to FIG. 3, a buffer layer 210 (diffusion barrier) is formed on a glass substrate 200 to prevent impurities such as metal ions diffused from the glass substrate 200 from infiltrating into

the activation layer of polycrystalline silicon.

[0032] An amorphous silicon layer is deposited on an upper part of the buffer layer 210 after forming the buffer layer 210. The dehydrogenated amorphous silicon layer is formed into polycrystalline silicon layer (polysilicon layer) through crystallization method such as ELA (excimer laser annealing), *etc.*, after dehydrogenating the amorphous silicon layer. Then, photoresist for forming an activation layer is formed on the polysilicon layer, and the activation layer 220 that functions as channel region of TFT (thin film transistor) is formed by patterning the polysilicon layer using the photoresist as a mask.

[0033] Next, the surface of the activation layer 220 is treated by a material such as HF to remove impurities including photoresist remaining on the surface of the activation layer 220 after the process of forming the activation layer 220.

[0034] A step A2 is formed on the buffer layer 210 due to over-etching of the buffer layer 210 during the activation layer forming process and activation layer surface treatment process. However, the step A2 is controlled in the present invention so that gate insulation layer is deposited to an even thickness on the side wall of the activation layer when subsequently depositing the gate insulation layer by controlling over-etching time of the buffer layer 210 during the activation layer forming process and activation layer surface treatment process.

[0035] The following Table 1 is a table showing a relation between thickness of the gate insulation layer 230 and step A2 caused by over-etching.

[0036] Table 1

Relation between thickness of the gate insulation layer and over-etching

Over etching	Thickness of Si	The maximum over etching value = (gate insulation layer+polysilicon thickness)/2	Destruction of TR	Gate insulation layer
500 Å	ELA 500 Å	750 Å	Action	Silicon oxide layer (1000 Å)
700 Å	ELA 500 Å	750 Å	Destruction initiation	
1000 Å	ELA 500 Å	750 Å	Destruction	
200 Å	SPC 300 Å	350 Å	Action	Silicon oxide layer (400 Å)
400 Å	SPC 300 Å	350 Å	Destruction initiation	

[0037] Referring to Table 1, it can be seen that a thin film transistor is destructed if step A2 having a height of 700 Å or more is formed by over-etching of buffer layer in case that thickness of ELA polysilicon layer used as activation layer 220 is 500 Å, and thickness of silicon oxide film that is gate insulation layer 230 is 1000 Å.

[0038] Furthermore, it can be also seen that the thin film transistor is destructed if step A2 having a height of 400 Å or more is formed by over-etching of buffer layer in case that thickness of SPC (solid phase crystallization) polysilicon layer that is an activation layer is 300 Å, and thickness of silicon oxide film that is gate insulation layer 230 is 400 Å.

[0039] That is, the thin film transistor is destructed if the step A2 formed by over-etching of the

buffer layer has a height corresponding to a half or more of the thickness sum of the gate insulation layer 230 and polysilicon layer as seen in the table 1 representing a relation between thickness of the gate insulation layer 230 and over-etching.

[0040] Therefore, it is preferable that step A2 of the buffer layer is formed in a height corresponding to a half or less of the thickness sum of the gate insulation layer 230 and polysilicon layer.

[0041] Subsequently, gate insulation layer 230 is formed on substrate equipped with the activation layer 220, a conductive gate metal is deposited on the upper part of the gate insulation layer 230, and gate electrode 240 is formed by patterning the gate metal.

[0042] The present invention provides a thin film transistor in which a short circuit is not generated between the activation layer and gate electrode by forming gate insulation layer to an even thickness on the side wall of the activation layer in case that the step is formed in a height corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer as illustrated in the above.

[0043] Furthermore, the present invention provides a thin film transistor capable of forming gate insulation layer more thinly and controlling thickness of activation layer also in advance by controlling the step.

[0044] While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.